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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,933	04/18/2006	Adrian Traskov	AP 10609	8562

52203 7590 03/27/2009

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EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2114	

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03/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,933	TRASKOV ET AL.	
	Examiner	Art Unit	
	JOSHUA A. LOHN	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/8/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Barlow, United States Patent number 3,789,204, published January 29, 1974.

As per claim 11, Barlow discloses a method for the detection and/or correction of memory access errors in a processor system, the method comprising: storing data which is to be secured in a memory (Barlow, col. 3, lines 61-63); and storing test data in the memory in addition to the data which is to be secured (Barlow, col. 4, lines 1-16, where the party bits are test data), wherein in addition to the data to be secured, addresses of the data are taken into account when generating the test data (Barlow, col. 4, lines 4-8).

As per claim 12, Barlow further discloses the method of claim 11, wherein the data to be secured is transmitted jointly with associated test data to a data receiver (Barlow, figure 1, where both the parity bits and the data are provided to a data receiver, element 1), and the test data is evaluated for error detection only after the data transfer (Barlow, col. 4, lines 23-28, where the data is evaluated for error detection when read)

As per claim 13, Barlow further discloses the method of claim 12, wherein the test data is evaluated for error detection in an error detection device that is checked by a checking unit

(Barlow, figure 1, where element 3 is the error detection device and element 10 is the checking unit).

As per claim 14, Barlow further discloses the method of claim 13 further comprising: generating further test data to check the error detection device by way of data supplied by the error detection device and the addresses of the data (Barlow, figure 1, where the address parity generator, element 9, provides further test data).

As per claim 15, Barlow further discloses the method of claim 13, wherein the checking unit produces comparative test data from data and addresses (Barlow, col. 4, lines 1-12) which are compared with at least test data of the error detection device or with test data of a memory connected to the error detection device (Barlow, col. 4, lines 23-31).

As per claim 16, Barlow further discloses the method of claim 13, wherein separate bus lines are used for the transmission of data, test data, and addresses between the error detection device and an application memory (Barlow, figure 1, where separate lines exist for transferring the parity test data, from element 2, data, from element 5, and address, from element 8).

As per claim 17, Barlow discloses an electronic circuit arrangement, for the detection and/or correction of memory access errors in a processor system, the electronic circuit arrangement comprising: an error detection device (Barlow, col. 4, lines 23-31); a processor core connected to the error correction device (Barlow, col. 1, line 18, where the memory is in a computer system, which inherently includes some form of processor core); and a memory connected to the error detection device, wherein the error detection device includes a test data

generator which generates test data for data to be stored in the memory by way of the data and addresses of the data (Barlow, col. 4, lines 1-13).

As per claim 18, Barlow further discloses the electronic circuit arrangement of claim 17, wherein the error detection device is connected to the memory by way of one or more bus lines (Barlow, figure 1, where the lines output from element 1 are the bus lines).

As per claim 19, Barlow further discloses the electronic circuit arrangement of claim 18, wherein separate bus lines are respectively provided for data, test data, and addresses (Barlow, figure 1, where the data, from element 1 to element 6, test data, from element 1 to element 3, and address, from element 8, are provided independent lines).

As per claim 20, Barlow further discloses the electronic circuit arrangement of claim 17, wherein a checking unit is associated with the error detection device (Barlow, figure 1, where the parity checker is the checking unit).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSHUA A. LOHN whose telephone number is (571)272-3661. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joshua A Lohn/
Primary Examiner, Art Unit 2114